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Baseband Processor Hardware for Advanced Communication Technology Satellite (ACTS)*

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Abstract

Motorola has developed a satellite baseband processor (BBP) for NASA Lewis Research Center's Advanced Communication Technology Satellite (ACTS) program. The objective of the ACTS program is to develop the high risk advanced communication technology required for future satellite systems and to promote effective utilization of the spectrum and growth in communication capacity.

Key features for this next generation satellite communication system include coverage of the contiguous United States through a control switching satellite in time-dimension, multiple-access (TDMA) mode. The use of Ka-band (30 GHz on the uplink and 20 GHz on the downlink) presents frequency reuse on a geographic basis because of the narrow beam scanning antenna.

The baseband processor developed by Motorola provides the flexible message routing capability needed to support the satellite's TDMA burst communications. Key technologies developed for the ACTS BBP included coherent serial minimum shift key (SMSK) burst demodulators, a family of high speed, low power large scale integrated (LSI) circuits, a maximum-likelihood convolutional decoder (MCD) on a single LSI chip, and the development of memory architectures using programmable control memories.

This paper gives a brief overview of the ACTS Multibeam communication package (MCP) payload, the Baseband Processor (BBP) subsystem description, baseband processor development history leading up to the ACTS BBP, and key technologies developed for the ACTS BBP. ACTS BBP functional description describing how hardware is partitioned into subassemblies (referred to as boxes) is presented.

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1. Introduction

The Advanced Communication Technology Satellite (ACTS) system consists of two major segments, the ground segment and the flight segment.

The Ground Segment consists of the Master Control Station (MCS), and the experimenters' terminals. The MCS located at NASA Lewis Research Center. The MCS controls the overall network traffic including response to traffic demands by the experimenters' terminals for capacity, responding to requests for fade protection and providing burst time plans to the BBP.

The Flight Segment (ACTS) is an experimental communication satellite that will demonstrate advanced technology.

The ACTS multibeam communication package (MCP) payload consists of three major advanced technology subsystems: The Multibeam Antenna (MBA), Baseband Processor (BBP), and IF switch matrix. A simplified block diagram of the MCP is shown in Figure 1. The MBA consists of receive and transmit Ka-band offset cassegrain antennas providing three fixed beams and two scanning beams. The hopping beams will independently, and simultaneously scan their sectors. The sectors will cover contiguous areas in the middle Atlantic and Great Lakes regions plus isolated spots in other regions of the United States. A lower gain, steerable antenna capable of being pointed anywhere within the hemisphere of ACTS field of view will cover Alaska and Hawaii.

The ACTS MCP will operate in two basic modes: A baseband processor mode and an IF switch mode. Both modes use a TDMA format with a 1-millisecond time frame. In the baseband processor mode two simultaneous and independent hopping beams provide flexible, demand-access low bit rate communications between small earth terminals. Bandwidth-efficient SMSK modulation will be used. Uplink bursts will be organized in frequency-division multiplexed TDMA format; downlink bursts will be time-division multiplexed.

The IF switch mode is based on satellite switched TDMA (SS/TDMA) and interconnects the three fixed beams and/or the hopping beams to support high bit rate communications associated with major metropolitan areas. The system is designed to operate at 220 Mbs, but other rates are possible. This mode does not restrict the ground terminals in their use of modulation techniques.

2. Baseband Processor (BBP)

Motorola has been developing advanced baseband processor technology for NASA for the last 8 years. From mid 1980 to mid 1983, Motorola developed the conceptual design and proof of concept (POC) Baseband Processor (BBP) for NASA's 30/20 GHz communication system (Ref. 1); the BBP POC is currently supporting system tests at NASA Lewis Research Center. The BBP Phase 2 program (1983 to mid 1985) developed nine large scale integrated (LSI) circuits needed to significantly reduce BBP size, weight, and power.

Motorola started the ACTS program in late 1984 and will deliver the flight BBP in mid 1989. A functional block diagram of the ACTS BBP is shown in Figure 2. The ACTS BBP represents a scaled down configuration with sufficient capability to demonstrate the baseband switching technology (Ref 2). The major BBP elements consist of two input channels, a 3×3 baseband routing switch, two output channels, and a central processor. The BBP supports a maximum data throughput of 220 Mbps.

Each input channel contains three dual rate SMSK demodulators, an input memory, data decoders, and control memories. The demodulators receive intermediate frequency (IF) inputs consisting of SMSK modulated IF bursts at approximately 3.2 GHz. Data bursts are received by either a 110/55 Mbps demodulator or by two 27.5/13.75 Mbps demodulators. Bursts received by the 110/55 Mbps demodulator occur uniquely in time relative to bursts received by the two 27.5/13.75 Mbps demodulators, with the higher rate demodulator sharing the IF channel with the two lower rate demodulators. The demodulator serial outputs are converted to 64-bit data words which are stored in an input data memory. Each input data memory stores 1728 64-bit words which supports a 1 millisecond frame of 110 Mbps data. In the case where uplink data bursts have been encoded to compensate for link degradation, the encoded messages are read from the input memory and shifted through parallel convolutional decoders to the routing switch. Unencoded data are conveyed directly to the routing switch. Input channel control memories generate control signals required by the demodulators for message acquisition, addresses for reading data memories, and control signals for decoding encoded data.

The 3×3 routing switch provides programmable routing at the full data throughput rate of 64-bit words from the input channels to the output channels. The 3×3 routing switch receives 110 Mbps serial data from the two input channels and from the central processor. These data streams are switched to either of the two output channels or to the central processor on a 64-bit word basis. An associated routing switch control memory operating at a rate of 110/64 megawords per second provides the routing switch interconnect instructions.

Each output channel contains an output memory, an encoder, a modulator and a control memory. An output channel receives 110 Mbps serial data from the routing switch and stores the data sequentially in the output memory. Downlink data formatting is provided by reading the output memory contents in a sequence determined by addresses programmed into the output control memory. When the downlink data stream does not require encoding it bypasses the encoder and is routed directly to the modulator. The downlink modulation rate is 110 Mbps per channel for unencoded data. Data requiring encoding are serially encoded prior to modulation. Half-rate encoding is performed at an input rate of 27.5 Mbps, producing an output symbol rate of 55 Msps for the downlink data.

The on-board central processor interfaces with the master control ground station either through a separate serial telemetry, tracking and command (TT&C) link or through the message uplink input channel via the routing switch. Commands from the master control station are processed by the central processor to update the various control memories causing message routing to be reprogrammed. System status data returned from the central processor allow the ground station to monitor Baseband Processor operation and to perform diagnostics.

3. ACTS BBP Hardware Description

The BBP is partitioned into three subassemblies: A Modem Box, an Input/Output Memory Box and a Central Processor Box. Figure 3 shows hardware partitioning and major functions for each box. Hardware partitioning emphasized critical interface signals and hardware integration and testing. The high speed baseband data interfaces are located between the Modem Box and the Input/Output Memory Box. The Central Processor Box manages all control memory update interfaces and the TT&C link interface.

The Modem Box contains 10 modules: Two modulator modules, six demodulator modules, and two power converters. The two modulator modules are single-sided shielded configurations with common modulator circuit designs occupying half of each module. The other half of the first module carries IF signal distribution circuitry, and the other half of the second module contains power converter control circuitry.

The Input/Output Memory Box contains 21 printed wiring boards (PWB's) and several shielded modules. Eleven PWB's make up the two input channels and 5 PWB's make up the two output channels. The routing switch function is redundant and occupies 4 PWB's. A redundant central timing function consists of one PWB and 2 shielded modules. Also, 4 power converter modules provide redundant power. A motherboard is used to interconnect low speed signals and power. A flexible coax harness is used to route high speed signals.

The Central Processor Box contains 14 PWB's, a relay and telemetry module, and a redundant pair of power converter modules. The Central Processor hardware is totally redundant with 7 PWB's containing one complete function. A motherboard is used to interconnect signals and power.

4. ACTS BBP Key Technologies

Several years of technology developments have led to the present implementation of the ACTS BBP. The key technologies developed for the ACTS BBP include: Rapid acquisition coherent SMSK burst demodulators operating from 27.5 Mbps to 110 Mbps; a family of high speed, low power LSI building block circuits; Forward error correction (FEC) utilizing a single chip maximum-likelihood convolutional decoder (MCD); modulator distributed processing techniques to implement the memory map concept of routing control; and a central processor architecture that provides satellite control via commands from the master control ground station.

SMSK Demodulator

Two dual rate SMSK demodulator designs support the 110 Mbps/55 Msps and 27.5 Mbps/13.75 Msps uplink data rates. Both use a common design approach as shown in Figure 4. A composite IF is received into a bandpass filter to limit adjacent channel interference. A variable gain amplifier provides 39 db of dynamic range at the input. An AGC feedback control provides a constant amplitude signal into the carrier tracking loop.

Each uplink burst is acquired separately. The data pattern at the start the uplink preamble assists the carrier tracking loop in acquiring the carrier frequency. The uplink preamble provides 204 bit periods for carrier acquisition for uncoded data, 110/27.5 Mbps, and 304 symbol periods for coded data .55/13.75 Msps. The preamble also provides for a rapid acquisition of the clock loop. A data pattern is injected into the clock loop pulling it to the correct frequency and phase. Clock injection is activated on the falling edge of Sync Gate Signal programmed into the demodulator control memory. During no message periods, a reference oscillator is switched into the loop to maintain a clock loop frequency.

The demodulator outputs are tied to an input memory assembly. Sign and magnitude data outputs are provided for two bit soft decision with the decoder. A Sync Up signal identifies coded symbol pair boundaries and helps establish a correlation window for uncoded data.

ACTS Custom LSI

A family of custom LSI circuits were developed for the ACTS BBP as listed in table 1. The LSI devices consist of complementary metal oxide semiconductor (CMOS) circuits and Motorola oxide self-aligned implanted circuits (MOSAIC). The MOSAIC circuits use both open collector current-mode logic (CML) and emitter coupled logic (ECL) to achieve the speed required for handling maximum-rate link data.

Table 1. ACTS Custom LSI Summary

Qty.	Function	Tech*	Processor Function Area
1. 4	Maximum-Likelihood Convolutional Decoder (MCD)	CMOS	Input Channel Decoding
2. 24	Memory Update Controller (MUC)	CMOS	Control Memories
3. 28	Serial-Parallel/Parallel-Serial	CMOS	Input Channel, Output Channel
4. 2	Encoder	M-ECL	Output Channel Encoding
5. 6	Serial to Parallel	M-CML	Input Channel
6. 32	Parallel to Serial	M-CML	Input Memory, Routing Switch, Output Channel
7. 6	Correlator	M-CML	Input Channel Synchronization
8. 4	Timing and Control A	M-CML	Input Channel Synchronization
9. 4	Timing and Control B	M-CML	Clock Distribution

*Semiconductor Technologies:
CMOS
MOSAIC-ECL
MOSAIC-CML

FEC Decoding

Convolutional decoding utilizing maximum-likelihood techniques is used in the ACTS BBP to provide forward error correction (FEC) to offset signal degradation caused by rain. A maximum-likelihood convolutional decoder (MCD) LSI was developed for the ACTS program (Ref. 3). The MCD implementation is a single-chip CMOS design using coding rate = 1/2, constraint length = 5, 2 bit soft decision and path memory length = 28. The MCD provides in excess of 4 dB of link improvement at a bit error rate of 10^{-6} relative to uncoded messages as shown in Figure 5. Coding rate = 1/2 coupled with a symbol rate reduction of one half provides an additional 6 dB gain for a total FEC improvement greater than 10 dB.

Sign and magnitude elements are generated by the demodulators from the coded symbols received and stored into the input memory. A coded word is read from the input memory on intervals of sixteen word times and loaded into parallel to serial converters for shifting through the decoders. Because of the decoder chip speed, parallel MCD chips are used to provide a total decoding throughput of 6.8 Mbps per channel. Odd and even coded symbol pairs are multiplexed into the parallel decoders as shown in Figure 6. Each decoder receives a sign and magnitude serial stream of 6.8 Msps generating a decoded output of 3.4 Mbps and the decoder outputs are multiplexed together.

Memory Architecture

The memory architecture shown in Figure 7 is used for both the input and output memories. This memory architecture provides a continuous store and forward function with a 110 Mbps throughput. Each frame time data is written into one data memory while the previous frame of data is read from the other. Data memories alternate read and write functions each frame.

The input and output memories receive high speed serial data from demodulator outputs and routing switch outputs respectively. Custom serial-to-parallel converter LSI's convert the high speed serial data into 64-bit words for storage into CMOS data memories. An incrementing counter provides sequential address for write operations and a control memory provides programmed address for read operations.

Control Memories

Control memories in the baseband processor direct data routing and control functions on a word-time basis repetitively each frame. All control memories are 2K deep allowing mapping of a full frame of 110 Mbps data on a 64-bit word basis. Control memories in the input channel generate control signals required by the demodulators for message acquisition, addresses for reading data memories and control signals for decoding coded data. A routing switch control memory controls interconnections through the 3×3 routing switch and directs the routing of central processor command and status words. Control memories in the output channels provide read-addresses and control signals for encoding.

Control memories are grouped in pairs such that one can actively control while the other is available to be programmed for new data routing configurations. Control memory update information is received from either the LBR uplink or the TT&C link, processed by the central processor and distributed to the control memories. Each control memory interfaces with the central processor through a memory update controller custom LSI. Memory update controllers receive serial update commands during the frame. Those controllers armed with data then transfer the data to their respective control memories during the last six 110 Mbps/64 word times at the end of a frame.

5. Conclusion

The BBP for NASA's Advanced Technology Satellite makes possible the interconnections necessary to support scanning spot beam LBR communications between many small earth terminals. The advanced technology developed for the BBP has resulted in a practical hardware implementation that meets payload size, weight, and power requirements necessary for an operational satellite system.

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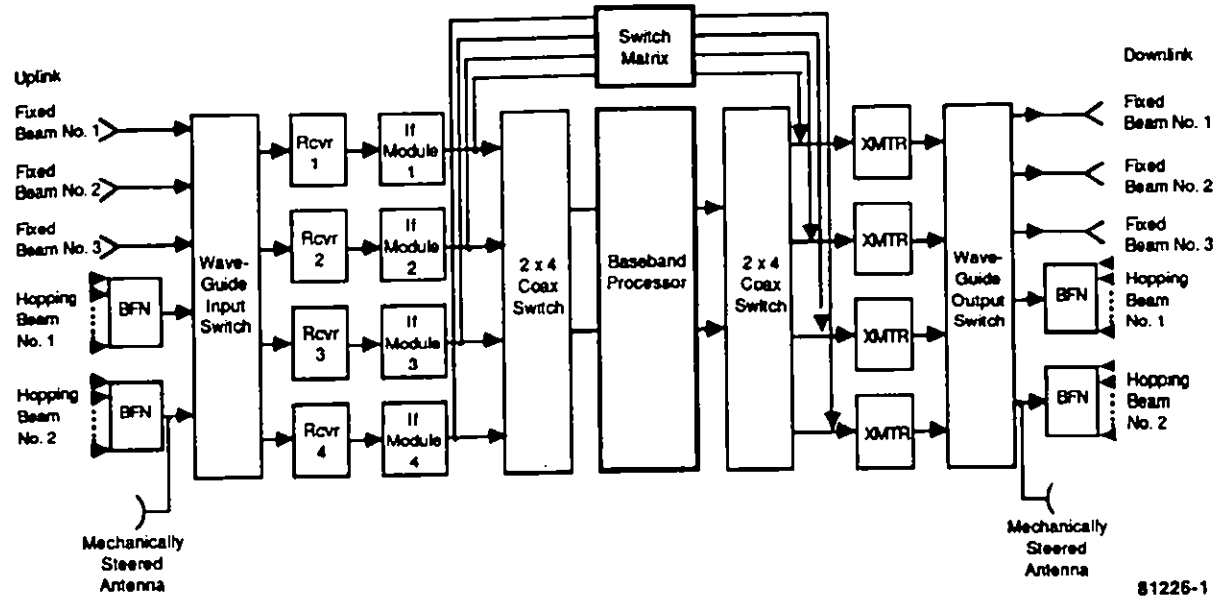

Figure 1. ACTS Multibeam Communication Package (MCP) Simplified Block Diagram

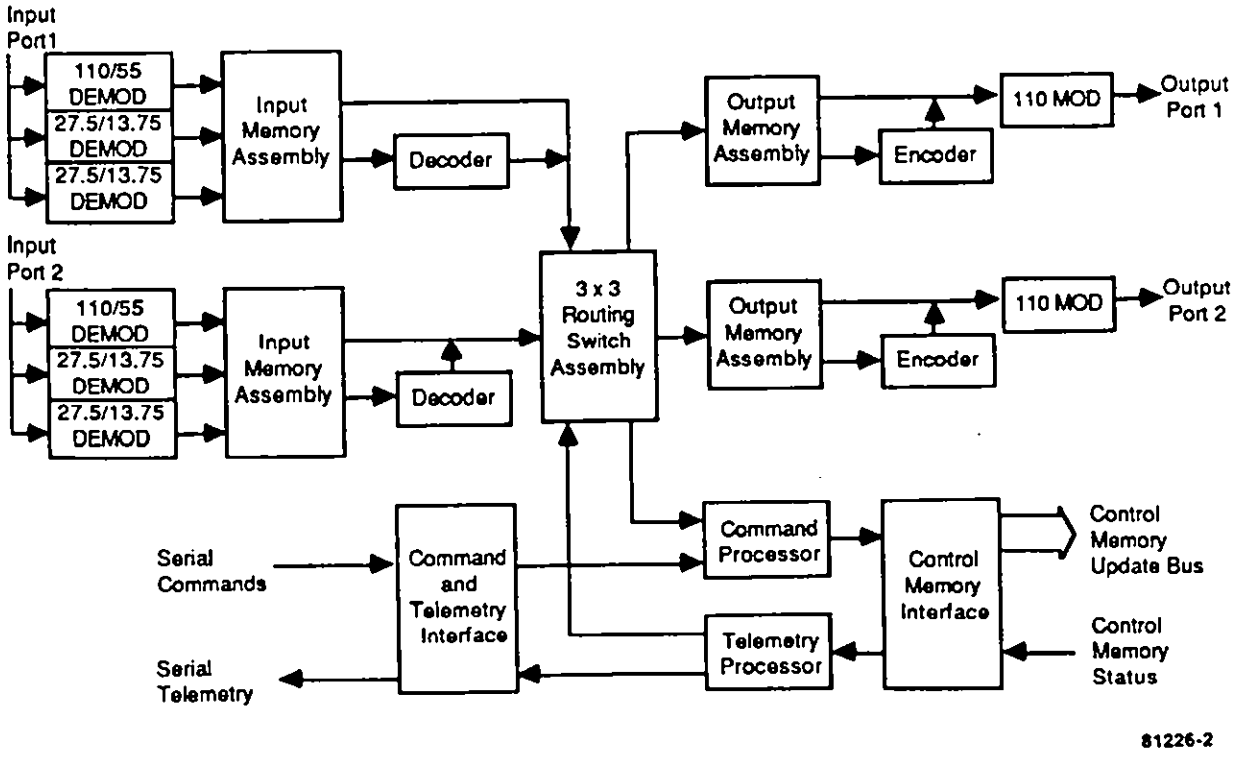

Figure 2. Baseband Processor Functional Block Diagram

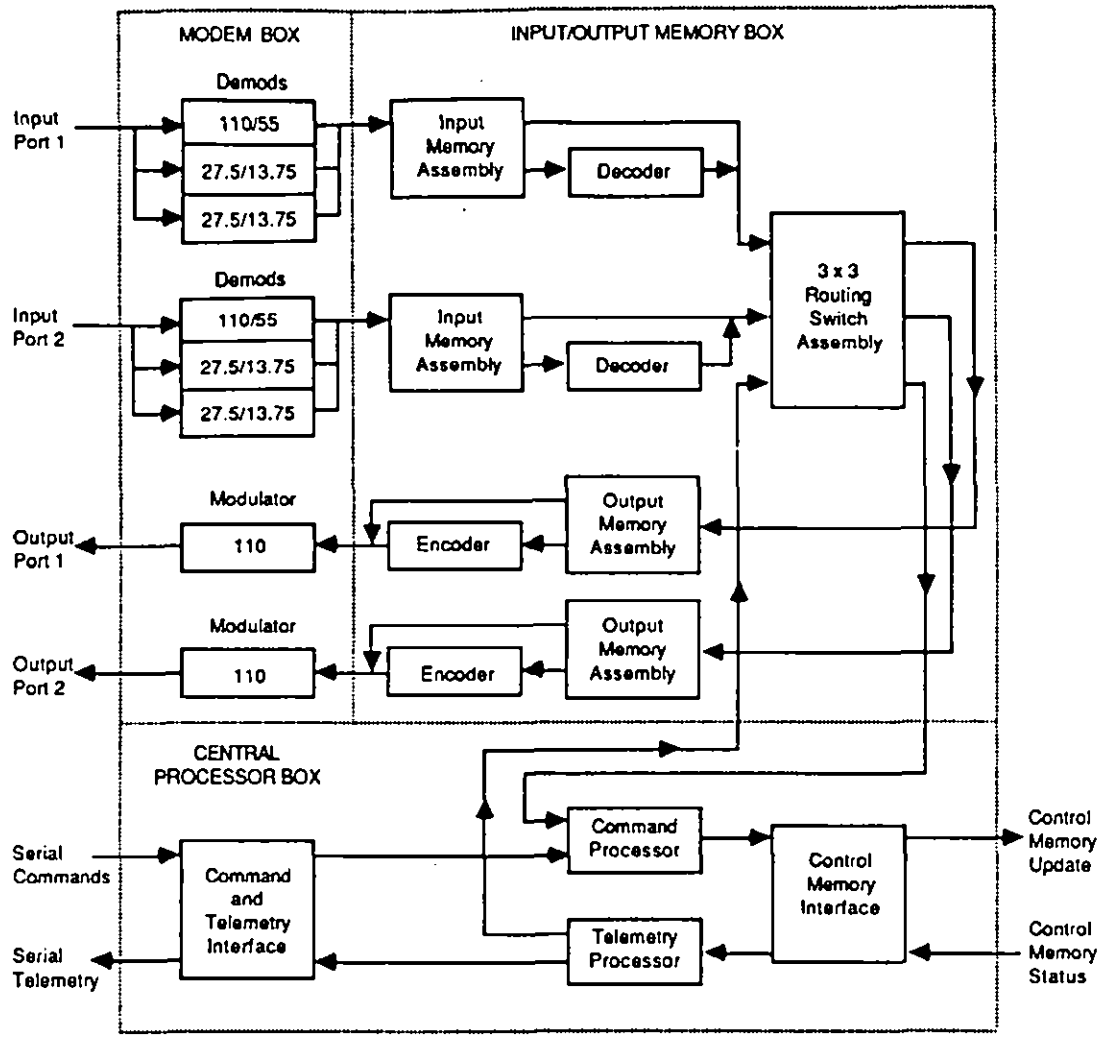

Figure 3. Baseband Processor Box Partitioning

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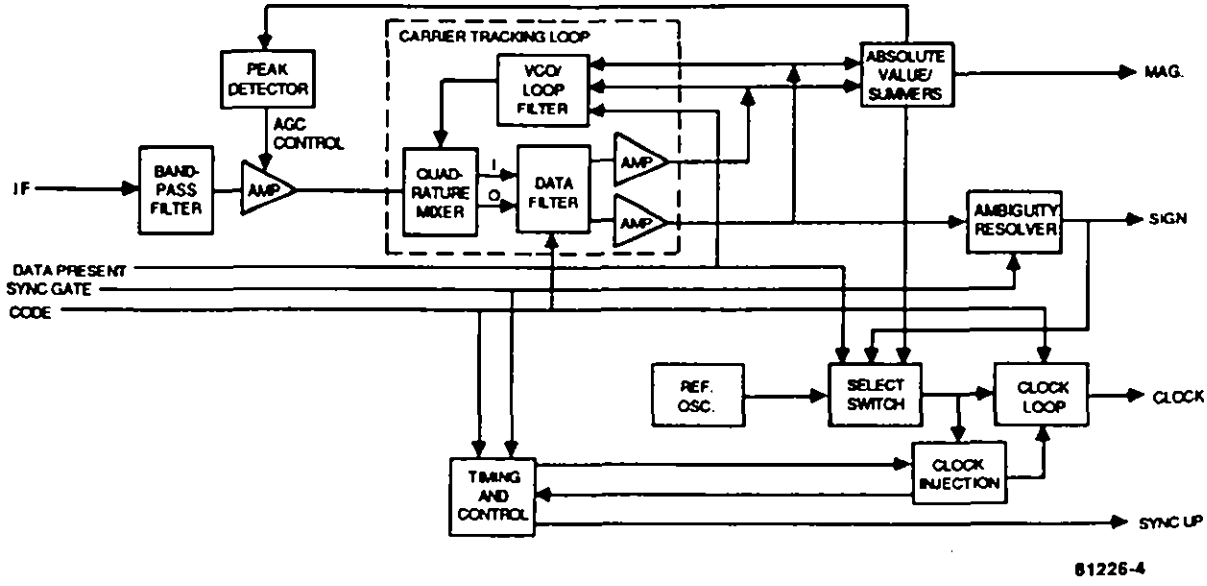

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Figure 4. SMSK Demodulator Functional Block Diagram

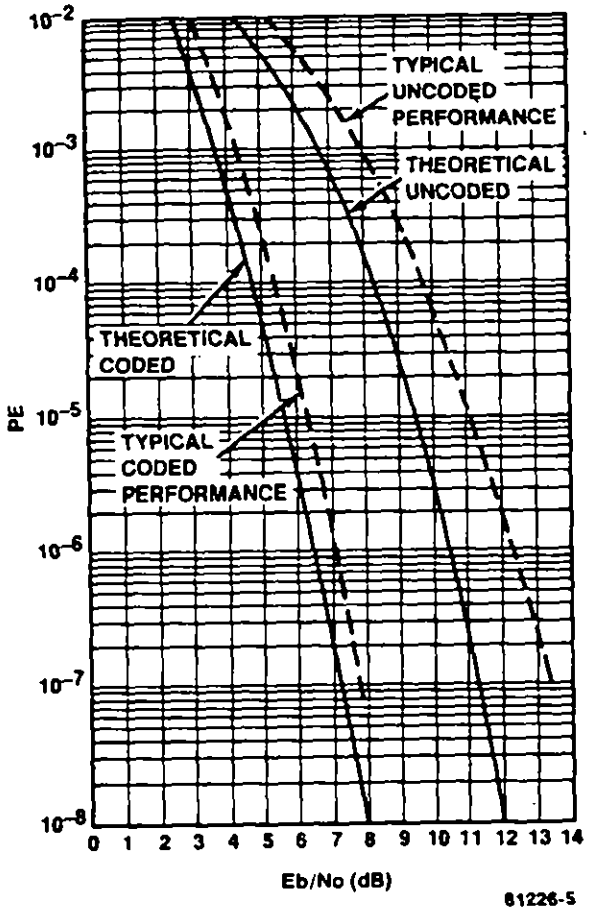

Figure 5. Coded and Uncoded BER Performance

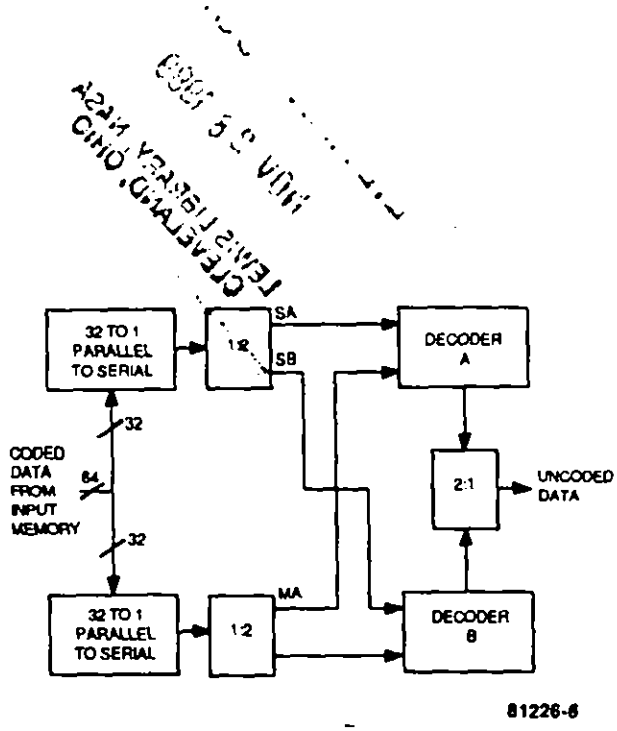

Figure 6. Input Channel Decoder Configuration

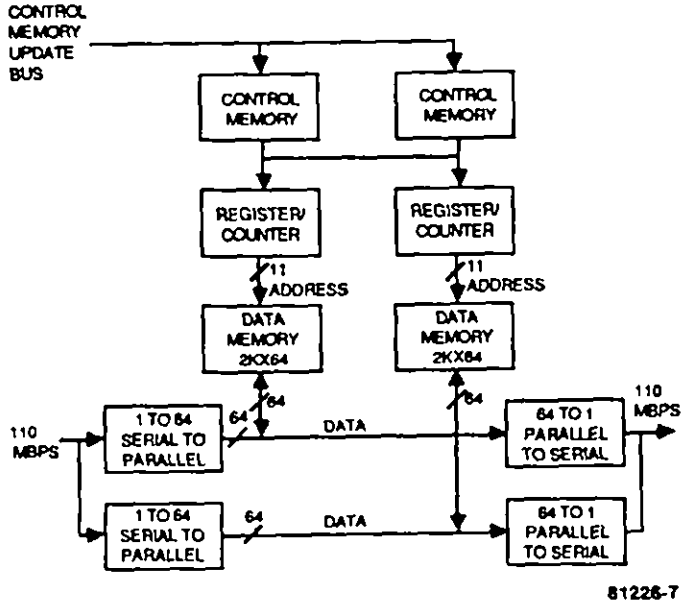

Figure 7. Memory Architecture